Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CURRENT SENSE**
2. **INPUT-**
3. **INPUT+**
4. **VREF**
5. **V-**
6. **NC**
7. **NC**
8. **VZ**
9. **VOUT**
10. **VC**
11. **V+**
12. **FREQ COMP**
13. **CURRENT LIMIT**

**.042”**

**.051”**

**13 12 11**

**4 5 8**

**10**

**9**

**1**

**2**

**3**

**MASK**

**REF**

**7**

**2**

**3**

**D**

**7**

**8**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 723D**

**APPROVED BY: DK DIE SIZE .042” X .051” DATE: 9/1/22**

**MFG: NATIONAL THICKNESS .013” P/N: LM723 MD8**

**DG 10.1.2**

#### Rev B, 7/19/02